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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/015,972	11/01/2001	Steven D. Roach	LT-146	6870

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EXAMINER	
TSAI, CAROL S W	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 03/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/015,972	ROACH, STEVEN D.	
	Examiner	Art Unit	
	Carol S Tsai	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/16/2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 17-40* is/are pending in the application.

4a) Of the above claim(s) *26-35* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,17-25 and 36* is/are rejected.

7)☒ Claim(s) *37-40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Election/Restrictions

2. This application contains claims 26-35 drawn to an invention nonelected without traverse in Mail Date 12/16/2003. A complete reply to the final rejection must include cancelation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3 and 36 are rejected under 35 U.S.C. 102(e) as being anticipated by U. S. Publication 2002/0050827 to Kronrod et al.

With respect to claims 1-3, Kronrod et al. disclose a method for determining a current supplied by an integrated circuit (see paragraphs 0010 and 0028) comprising: determining a

voltage drop across a termination impedance with respect to a reference voltage (see paragraph 0039); comparing a voltage drop across a first impedance on the integrated circuit with a voltage drop across a second impedance on the integrated circuit, wherein the first impedance is different from the second impedance (see paragraphs 0034-0038); and processing information obtained in the determining and comparing steps to obtain a value for the supplied current (see paragraph 0040-0043).

As to claim 36, Kronrod et al. also disclose determining an impedance value of the first impedance, an impedance value of the second impedance, the voltage provided by the voltage reference, and the impedance value of the termination impedance (see paragraphs 0037, 0038, and 0047).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 17-19, 22, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,451,903 to Armstrong in view of U. S. Publication 2002/0050827 to Kronrod et al.

With respect to claims 17-19, 22, and 25, Armstrong discloses a circuit that determines a current supplied by an integrated circuit comprising: a sensing impedance (a control resistor 220 shown on Fig. 3) disposed on the integrated circuit (output driver 100 shown on Fig. 3); a

modulation impedance (impedance element 120 shown on Fig. 3); a termination impedance (external impedance load 160 shown on Fig. 3).

Armstrong does not disclose a first measurement device coupled to the modulation and sensing impedances configured to measure voltage drop across each impedance; a second measurement device coupled to the termination impedance configured to measure voltage drop across the termination impedance; and processing circuitry configured to receive information from the first and second measurement devices and calculate supplied current therefrom.

Kronrod et al. teach a first measurement device (A/D convert 218 shown on Fig. 5a) coupled to the modulation and sensing impedances configured to measure voltage drop across each impedance; a second measurement device (A/D convert 218 shown on Fig. 5a) coupled to the termination impedance configured to measure voltage drop across the termination impedance; and processing circuitry (CPU 220 shown on Fig. 5a) configured to receive information from the first and second measurement devices and calculate supplied current therefrom (see paragraphs 0041 and 0042).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Armstrong's system to include a first measurement device coupled to the modulation and sensing impedances configured to measure voltage drop across each impedance; a second measurement device coupled to the termination impedance configured to measure voltage drop across the termination impedance; and processing circuitry configured to receive information from the first and second measurement devices and calculate supplied current therefrom, as taught by Kronrod et al., in order to output corresponding digital signals (V2' and V reference) which may be input into CPU 220 or other calculation means in order

to perform the power calculations (see Kronrod et al., paragraph 0047, lines 12-15).

8. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Armstrong in view of Kronrod et al. as applied to claim 17 above, and further in view of U. S. Publication 2003/0006747 to Jaussi et al.

As noted above, Armstrong in combination with Kronrod et al. teach all the features of the claimed invention, but do not disclose a trimmed voltage reference.

Jaussi et al. teach a trimmed voltage reference (see paragraphs 0022 and 0066).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Armstrong in combination with Kronrod et al.'s system to include a trimmed voltage reference, as taught by Jaussi et al., in order to bias the variable current sources.

9. Claims 21, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Armstrong in view of Kronrod et al. as applied to claim 17 above, and further in view of U. S. Patent No. 5,687,330 to Gist et al.

As noted above, Armstrong in combination with Kronrod et al. teach all the features of the claimed invention, but do not disclose the termination impedance being a precision resistor.

Gist et al. teach the termination impedance being a precision resistor (see col. 14, lines 22-39).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Armstrong in combination with Kronrod et al.'s system to include

the termination impedance being a precision resistor, as taught by Gist et al., in order to compensate for electrical variations caused by aging, temperature, supply voltage and process variations (see Gist et al. col. 14, lines 31-32).

As to claim 23, Armstrong in combination with Kronrod et al. do not disclose the termination resistor being a resistor internal to the integrated circuit.

Gist et al. teach the termination resistor being a resistor internal to the integrated circuit (see col. 8, lines 6-15).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Armstrong in combination with Kronrod et al.'s method to include the termination resistor being a resistor internal to the integrated circuit, as taught by Gist et al., in order that signal amplitude can be automatically calibrated based on a precise electrical reference.

As to claim 24, Armstrong also disclose a sinking circuit (sinking transistor 226 shown on Fig. 3) coupled to the modulation resistor.

Allowable Subject Matter

10. Claims 37-40 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

11. Applicant's arguments filed 12/16/2003 have been fully considered but they are not persuasive.

Applicant argues that Kronrod et al. neither shows or suggests a method for measuring current supplied by an integrated circuit because Kronrod et al. is directed to measuring the power consumed by an integrated circuit on a PCB, that the Examiner has not identified any motivation or suggestion in Kronrod to measure the output current of an integrated circuit. The Examiner disagrees with Applicant. As set forth above, Kronrod et al. do disclose a system for measuring the core power of a circuit on a printed circuit board (PCB) which has a load (load 208 shown on Fig. 4) that are external to an integrated circuit, including a power source 202 (VDC1), such as a DC voltage source, which supplies power to a power plane 204 via a power strip 206 (e.g., a wide copper strip) wherein the power plane 204 is used to supply power to a circuit 208, which has a predetermined load (see Fig. 4 and paragraphs 0028 and 0034).

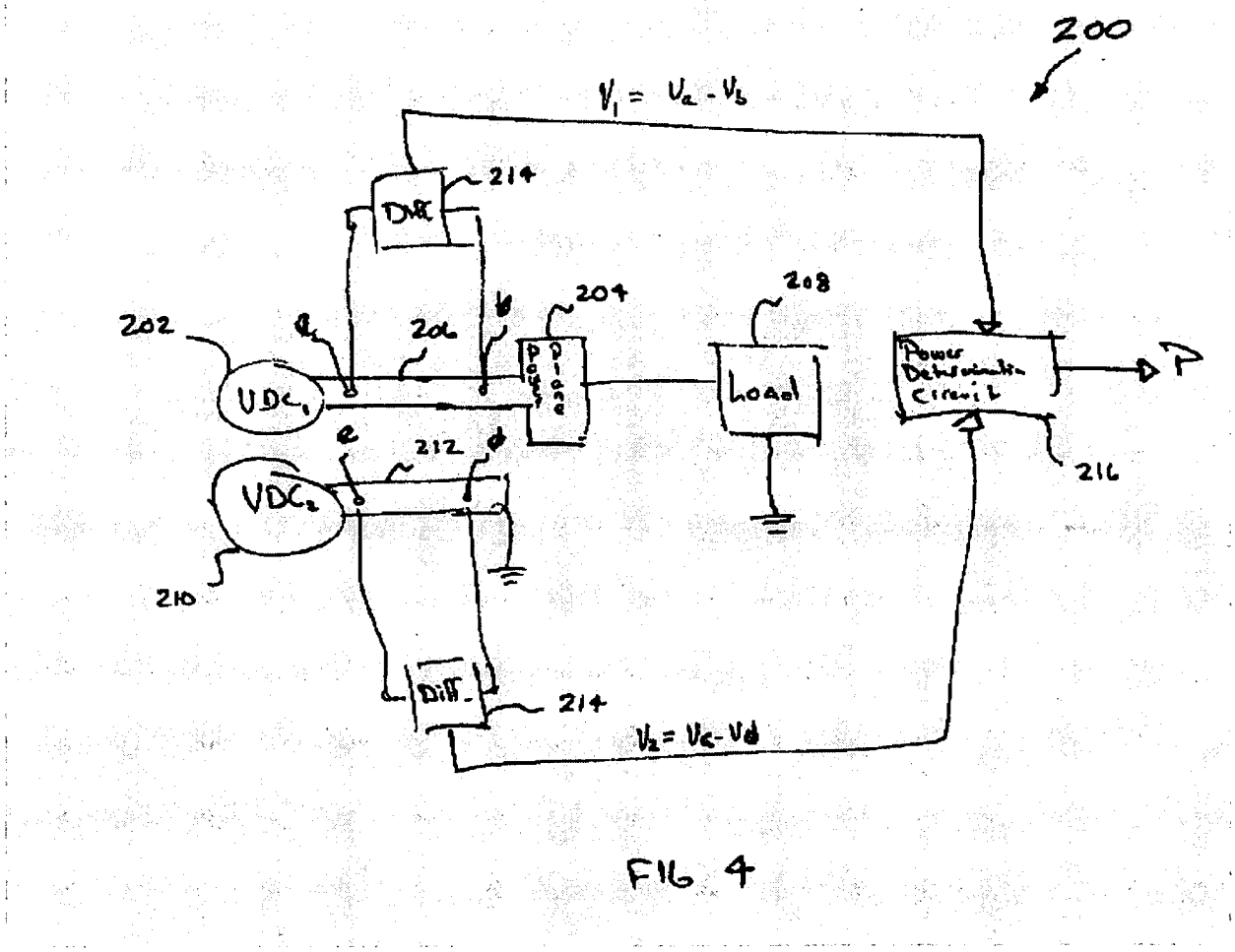

FIG 4

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Armstrong discloses an output driver for driving an external impedance load

comprising an output stage for controlling an input signal to drive the external impedance load, and an impedance element for coupling a voltage supply to the output stage. Kronrod et al. disclose a system for measuring the core power of a circuit on a printed circuit board (PCB) which has a load that are external to an integrated circuit, including a power source, such as a DC voltage source, which supplies power to a power plane via a power strip (e.g., a wide copper strip) wherein the power plane is used to supply power to a circuit, which has a predetermined load. As set forth above, Armstrong disclose claimed invention except for a first measurement device coupled to the modulation and sensing impedances configured to measure voltage drop across each impedance; a second measurement device coupled to the termination impedance configured to measure voltage drop across the termination impedance; and processing circuitry configured to receive information from the first and second measurement devices and calculate supplied current therefrom. Kronrod et al. teach a first measurement device coupled to the modulation and sensing impedances configured to measure voltage drop across each impedance; a second measurement device coupled to the termination impedance configured to measure voltage drop across the termination impedance; and processing circuitry configured to receive information from the first and second measurement devices and calculate supplied current therefrom, in order to output corresponding digital signals (V2' and V reference) which may be input into CPU 220 or other calculation means in order to perform the power calculations. Therefore, the combination of Armstrong and Kronrod et al. clearly teach the claimed invention.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carol S. W. Tsai whose telephone number is (571) 272-2224. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (571) 272-2216. The fax number for TC 2800 is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC 2800 receptionist whose telephone number is (571) 272-1585 or (571) 272-2800.

In order to reduce pendency and avoid potential delays, Group 2800 is encouraging FAXing of responses to Office actions directly into the Group at (703) 872-9306. This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2800 will be promptly forwarded to the examiner.

Carol S. W. Tsai

02/27/04

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